producing the result that the transfer of the film can be smoothed and the recording noise can be decreased.

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) An image recording method of recording a single pixel forming an image using a plurality of pulses comprising the step of:

expressing gradation using a first pulse expressing a superordination bit having a larger pulse width and a second pulse expressing a subordination bit having a smaller pulse width.

2. (Amended) The image recording method according to claim 1, said first pulse expressing said superordination bit having said larger pulse width lying at irregular intervals applied to said single pixel.

3. (Amended) An image recording method of recording a single pixel forming an image using a plurality of pulses, comprising the step of:

having activation or non-activation operation for each of said pulses, related to a specified bit forming image data.

4. (Amended) An image recording method comprising the steps of:

expressing gradation using a first pulse having a larger pulse width expressing a superordination bit and a second pulse having a smaller pulse width expressing a subordination bit; and

having activation or non-activation operation for each of said pulses, related to a specified bit forming image data.

5. (Amended) An image recording apparatus comprising:

an image recording unit which records an image in a first direction;

a transfer unit which relatively transfers said image recording unit and a recording medium in a second direction normal to said first direction; and

a record control unit which controls and records a single pixel using a plurality of pulses when said image is recorded, said record control unit expressing gradation for said image to be recorded using a first pulse having a larger pulse width expressing a superordination bit and a second pulse having a smaller pulse width expressing a subordination bit.

Cont.

6. (Amended) The image recording apparatus according to claim 5, said first pulse expressing said superordination bit having said larger pulse width lying at irregular intervals applied to said single pixel.

7. (Amended) An image recording apparatus comprising:

an image recording unit which records an image in a first direction;

a transfer unit which relatively transfers said image recording unit and a recording medium in a second direction normal to said first direction; and

a record control unit which controls and records a single pixel using a plurality of pulses when said image is recorded, said record control unit having activation or non-activation operation for each of said pulses, related to a specified bit forming image data.

8. (Amended) An image recording apparatus comprising:

an image recording unit which records an image in a first direction;

a transfer unit which relatively transfers said image recording unit and a recording medium in a second direction normal to said first direction; and

a record control unit which controls and records a single pixel using a plurality of pulses when said image is recorded, said record control unit expressing gradation for said image to be recorded using a first pulse having a larger pulse width expressing a superordination bit and a second pulse having a smaller pulse width expressing a subordination bit, and having activation or non-activation operation for each of said pulses, related to a specified bit forming image data.

Please add the following new claims:

--12. (New) The apparatus of claim 5, said record control unit comprising:

a controller that generates a plurality of timing signals that are transmitted to respective frequency dividers to generate said plurality of pulses, wherein at least one of said frequency dividers outputs a first frequency divided signal to a switching device, and at least another of said frequency dividers outputs a second frequency divided signal to a processing circuit that generates at least one output in accordance with stored data.--

--13. (New) The apparatus of claim 12, wherein said processing circuit generates outputs to respective ones of a plurality of line memory devices, each of which generates a line memory pulse in accordance with a clocking signal received from said controller.--

--14. (New) The apparatus of claim 13, wherein said line memory pulse of each of said line memory devices is input to said switching device, which selects said line memory pulse from one of said line memory devices, and forwards said selected line memory pulse to said image recording unit.--

--15. (New) The method of claim 1, further comprising:

generating a plurality of timing signals that are transmitted to respective frequency dividers to generate said plurality of pulses;

at least one of said frequency dividers outputting a first frequency divided signal to a switching device, and at least another of said frequency dividers outputs a second frequency divided signal to a processing circuit; and

said processing circuit generating at least one output in accordance with stored data.--

--16. (New) The method of claim 15, wherein said generating step comprises generating outputs to respective ones of a plurality of line memory devices, each generating a line memory pulse in accordance with a clocking signal received from said controller.--

--17. (New) The method of claim 16, further comprising: inputting said line memory pulse of each of said line memory devices into said switching device; and

said switching device selecting said line memory pulse from one of said line memory devices, and forwarding said selected line memory pulse to said image recording unit.--

--18. (New) The apparatus of claim 7, wherein a pattern of generating said plurality of pulses is set to be random between the pixel positions in a horizontal direction to prevent cyclic irregularity.--

--19. (New) The method of claim 1, wherein thermal patterns are made to be different between at least one neighboring pixels and neighboring lines of image data.--

--20. (New) The apparatus of claim 5, said record control unit comprising a data storage unit that stores data indicative of the correlation between said superordination bit and said first pulse, and said subordination bit and said second pulse .--

Q'10 cont.

--21 (New). The method of claim 1, wherein a gradation of N levels is expressed using fewer than N-1 pulses.--

--22 (New). The method of claim 3, wherein a gradation of N levels in said single pixel is expressed using fewer than N-1 pulses.--